

CLAIMS

What is claimed is:

1 1. A method comprising:
2 forming a first via; and
3 stacking a second via onto the first via, at least one of the first via and the
4 second via being a skip via.

1 2. The method of claim 1 wherein stacking a second via onto the
2 first via includes stacking a second skip via onto a first skip via.

1 3. The method of claim 1 wherein stacking the second via onto the
2 first via includes substantially aligning a longitudinal axis of the first via with a
3 longitudinal axis of the second via.

1 4. The method of claim 1 wherein forming a first via comprises:
2 forming a first conductive layer onto a core;
3 forming a first dielectric layer such that the first conductive layer is
4 between the first dielectric layer and the core;
5 forming a second conductive layer onto the first dielectric layer;
6 forming a second dielectric layer such that the second conductive layer is
7 between the first dielectric layer and the second dielectric layer;
8 forming an opening in the first and second dielectric layers; and
9 forming a first skip via in the opening.

1 5. The method of claim 4 wherein forming an opening in the first
2 and second dielectric layers includes drilling an opening in the first and second
3 dielectric layers.

1 6. The method of claim 5 wherein drilling an opening in the first and
2 second dielectric layers includes laser drilling an opening in the first and second
3 dielectric layers.

1 7. The method of claim 4 wherein forming an opening in the first
2 and second dielectric layers includes etching an opening in the first and second
3 dielectric layers.

1 8. The method of claim 4 wherein forming a first conductive layer
2 includes plating the first conductive layer onto the core and patterning the first
3 conductive layer, and wherein forming a second conductive layer includes
4 plating the second conductive layer onto the first dielectric layer and patterning
5 the second conductive layer.

1 9. The method of claim 4 wherein forming the first skip via in the
2 opening includes filling the opening with a conductive material.

1 10. The method of claim 9 wherein filling the opening with a
2 conductive material includes forming a third conductive layer onto the second
3 dielectric layer.

1 11. The method of claim 4 wherein forming a third conductive layer
2 on the second dielectric layer includes patterning the third conductive layer.

1 12. The method of claim 10 further comprising:
2 forming a third dielectric layer on the third conductive layer;
3 forming a second opening in the third dielectric layer; and
4 forming the second via in the second opening.

1 13. The method of claim 12 wherein forming the second via in the
2 second opening includes forming a fourth conductive layer onto the third
3 dielectric layer.

1 14. A substrate comprising:
2 a plurality of dielectric layers;
3 a first skip via extending through two of the dielectric layers; and
4 a second via extending through one of the dielectric layers, the second
5 via and the first skip via being stacked on top of one another.

1 15. The substrate of claim 14 wherein the second via is a second skip
2 via extending through two of the dielectric layers.

1 16. The substrate of claim 14 wherein the first skip via includes a
2 longitudinal axis and the second via includes a longitudinal axis, the longitudinal
3 axis of the first skip via being substantially aligned with the longitudinal axis of
4 the second via.

1 17. The substrate of claim 14 further comprising a third via extending
2 through at least one of the dielectric layers, the third via being stacked onto the
3 first skip via and the second via.

1 18. The substrate of claim 14 wherein the plurality of dielectric layers
2 is formed on a core.

1 19. A computer system comprising:
2 a bus;
3 a memory coupled to the bus; and
4 a substrate electrically coupled to the bus, the substrate including a
5 plurality of dielectric layers, a first skip via extending through two of the
6 dielectric layers and a second via extending through one of the dielectric layers,
7 the second via and the first skip via being stacked on top of one another.

1 20. The computer system of claim 19 wherein the second via is a
2 second skip via extending through two of the dielectric layers.

1 21. The computer system of claim 19 further comprising a processor
2 coupled to the substrate and the bus.